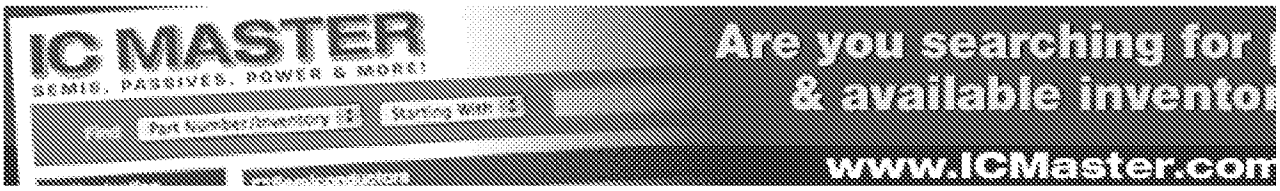

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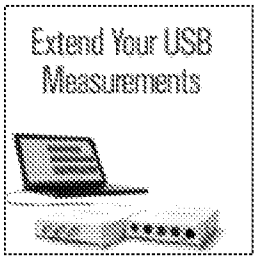

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NAND vs. NOR flash technology

The designer should weigh the options when using flash memory

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NOR and NAND technologies dominate today's nonvolatile flash memory market. NORflash, first introduced by Intel in 1988, revolutionized the market formerly dominated by EPROM- and EEPROM-based devices.

The introduction of Toshiba's NAND flash architecture in 1989, addressed the need for lower cost per bit, higher-performance, and disklike memory with a consistent interface for easy upgrade. Over a decade later, most hardware engineers are still not familiar with the differences between NOR and NAND flash technologies.

The phrase "flash memory" often is used interchangeably with the phrase "NOR-based memory." Many in the industry are unaware of the competing NAND flash technology and its advantages over NOR because most flash devices are used to store and run small amounts of code--for which NOR flash is more suitable. NAND is an ideal solution for high-capacity data storage, as can be seen in the *table*.

A feature of NOR is eXecute In Place (XIP), which allows an application to be run directly from flash instead of reading the application code into system RAM. NOR delivers high read performance and is most cost effective in lower capacities--1 to 4 Mbytes--but suffers from extremely low write-and-erase performance.

NAND architecture competes by offering extremely high cell densities that translate to high storage capacity, combined with

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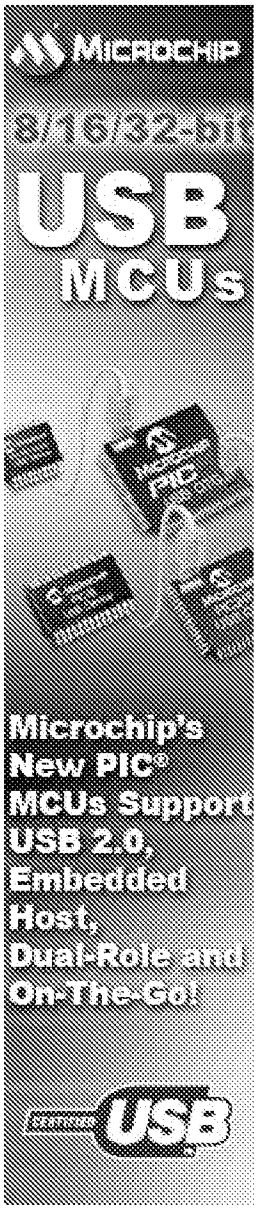


fast write and erase rates. The difficulty using NAND revolves around the need for flash management and special requirements for system interface.

Performance

Flash memory is nonvolatile memory that can be erased and reprogrammed in unitsof memory called blocks. A write operation in any flash device can only be performed on an empty/erased unit, so in most cases an erase operation must precede the write operation. The erase operation is fairly straightforward for NAND devices, whereas NOR technology mandates that all bytes in the target block be written with zeros before they can be erased.

Since the size of an erase block in NOR ranges from 64 to 128 Kbytes, such a write/erase operation can take up to 5 s. By contrast, using erase blocks 8 to 32 Kbytes in size, NAND performs the identical operation in a maximum of 4 ms.

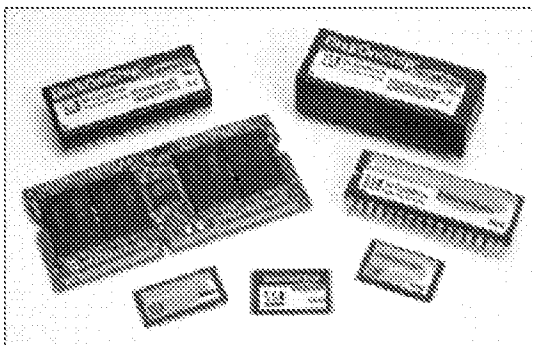
The erase block-size difference further increases the performance gap between NOR and NAND, as statistically more erase operations must be performed in NOR-based units per any given set of write operations (especially when updatingsmall files). Therefore, when selecting a local storage solution, designers need to weigh the following factors:

- NOR reads slightly faster than NAND.
- NAND writes significantly faster than NOR.
- NAND erases much faster than NOR--4 ms vs. 5 s, respectively.
- Most writes require a preceding erase operation.
- NAND has smaller erase units, so fewer erases are needed.

Interface differences

NOR flash has an SRAM interface. It has enough address pins to map its entire media, allowing for easy access to every byte contained in it.

NAND devices are accessed serially via a complicated I/O interface, which may vary from one device or vendor to another. The same eight pins are used to convey control, address, and data information.



Some NAND-based flash disks, like M-Systems' DiskOnChip products, use on-chip drivers to deliver the benefits of both

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NAND and NOR technologies.

NAND read-and-write operations occur in bursts of 512 bytes, which is similar to how hard drives manage these operations. This positions NAND-based memory tobe a logical choice to use for hard drive or block-device replacement.

Capacities and cost

The cell size of NAND flash is almost half the size of a NOR cell. In combination with a simpler production process, NAND architecture can be offeredwith higher capacity for a given die size, resulting in a lower price tag.

NOR flash dominates the market in memory capacity ranging between 1 and 16 Mbytes, while NAND flash is used in capacity ranges between 8 to 128 Mbytes. This again stresses the roles of NOR devices as a code-storage media and NAND devices as ideal for data storage--NAND has its strongest market presence in the memory card market (CompactFlash, Secure Digital, PC Cards, and MMC).

Reliability and endurance

One of the main considerations of working with flash media is its reliability. Flash is the preferred storage solution for systems in need of extended MTBF. Comparison of reliabilities between NOR and NAND architectures breaks down intothree main factors--life span (endurance), bit flipping, and bad-block handling.

Life span (endurance)

The maximum allowed number of erase cycles per erase block in a NAND device is one million cycles, compared with 100,000 cycles for a NOR device. In addition to the 10-to-1 block-erase-cycle advantage of NAND memory devices, the typical NAND block size itself is about 8 times smaller than that of a NOR device--eachNAND memory block will be erased fewer times over a given period of time.

Bit flipping

All flash architectures today suffer from a phenomenon known as "bit flipping."On some occasions (rare, yet more common in NAND than in NOR), a bit either gets reversed or is reported reversed.

One bit change may seem insignificant, but this minor glitch may hang the system altogether if it corrupts a critical file. When the problem is just one of reporting, repeating the read operation may solve it.

However, if the bit has actually been changed, an error detection/error correction (EDC/ECC) algorithm must be applied. Problems associated with bit flipping are more common with NAND devices than NOR and all NAND vendors now recommend

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using an EDC/ECC algorithm with their devices.

This problem is not as critical when using NAND to store multimedia information. However, when used as a local storage device storing the operatingsystem, configuration files, or other sensitive information, an EDC/ECC system must be implemented to ensure reliability.

Bad-block handling

NAND devices are shipped with bad blocks randomly scattered within them. An early attempt to ship NAND devices free of bad blocks was found not to be economically practical due to the very high price tag caused by low-production yield rates.

NAND devices require an initial scanning of the media for bad blocks, which aremapped as unusable. Failing to perform this process in a reliable way results in high-failure rates in the finished device.

Ease of use

Using a NOR-based flash is a straightforward process. It is connected like other memory devices, and code can be run directly from it.

NAND, however, is complicated with its requirement for an I/O interface. Accessing rules for NAND interfaces may differ depending on the NAND vendor.

A driver must be written and used for performing any operation on a NAND device. Writing information to a NAND device is a particularly tricky issue, since the designer must not write to a bad block--meaning that virtual mapping must be implemented on NAND devices at all times.

Software support

When discussing software support, two levels of support are distinguished: basic for read/write/erase operations and high level software for disk emulation and flash management algorithms--including performance optimization.

Running code *from* NOR devices requires no special software support. Doing the same thing in NAND requires a driver, usually referred to as a memorytechnology driver (MTD). Both NAND and NOR require MTDs for write and erase operations.

Working with NOR does not require much more than MTDs. Higher-level software isavailable for NOR devices from many vendors, including M-Systems' TrueFFS drivers--used by vendors such as Wind River Systems, Microsoft, QNX Software Systems, Symbian, and Intel.

The drivers also implemented in the company's DiskOnChip

products provide both disk emulation and NAND flash management, including bit-error correction, bad-block handling, and wear leveling.

NOR-NAND comparison

PARAMETER	NOR	NAND
Capacity	1 to 16 Mbytes	8 to 128 Mbytes
XIP (code execution)	Yes	No
Performance Erase Write Read	 Very Slow (5 s) Slow Fast	 Fast (3 ms) Fast Fast
Strengths	Addressable to every byte	More than 10% higher life expectancy
Erase cycle range	10,000 to 100,000	100,000 to1,000,000
Interface	SRAM-like, memory mapped	Accessed in bursts of 512 bytes; I/O mapped
Access method	Random	Sequential
Price	High	Very low

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